

Hardware Unit Test Report

Power Sequence Test

Hardware version	FW version	Sample No.	eMMC Flash P/N
V125	19.531.13	S/N: TBD	DDR: 1. K4A8G165WC-BCTD 2. K4A4G165WF-BCTD eMMC: KLM8G1GETF-B041

1. Power Test Setup

Equipment:

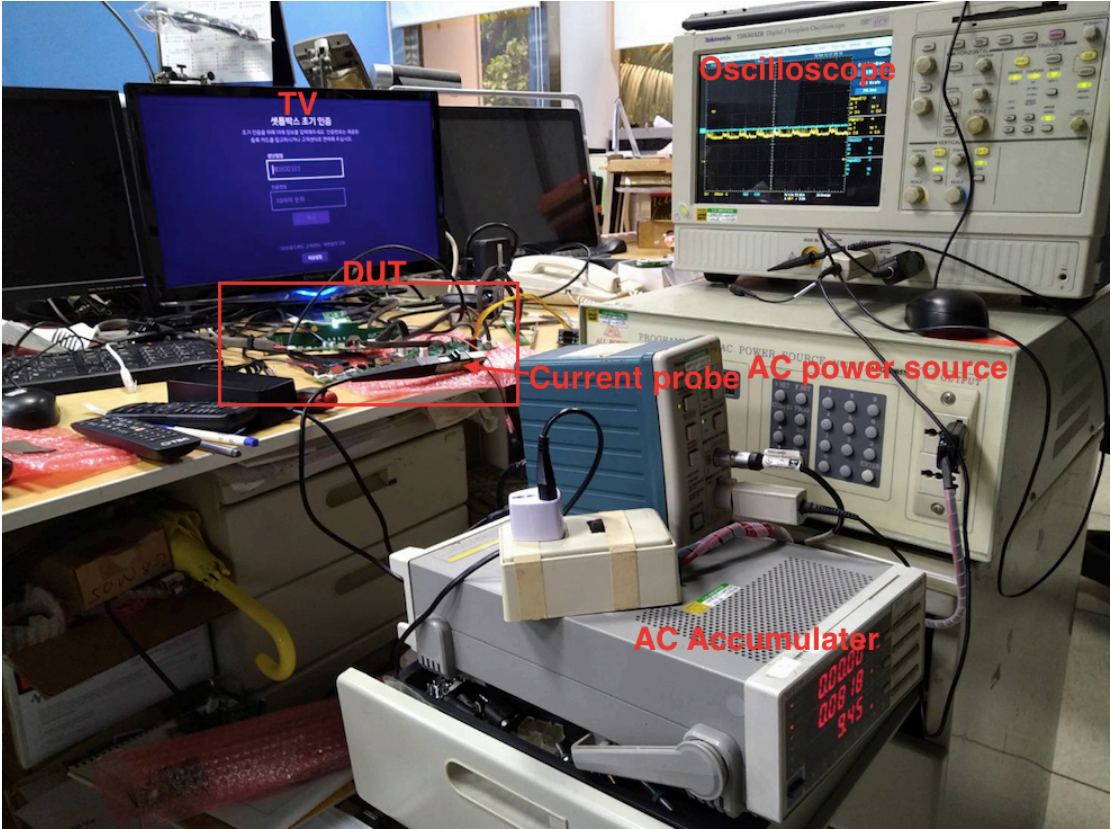
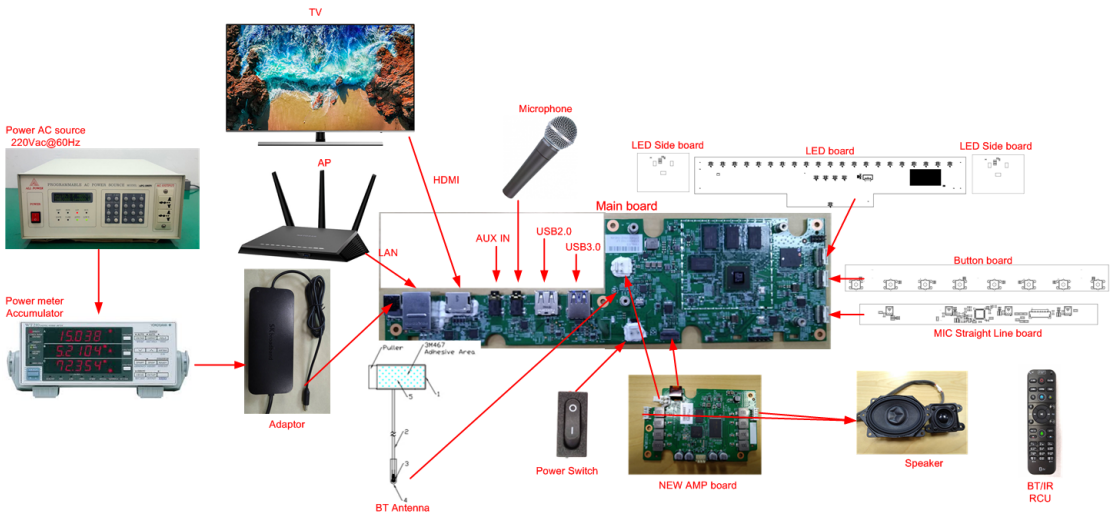
1. BFX-UA300 DVT board V125.
2. AC POWER: APG-1005N: 220Vac @60Hz
3. AC Adapter: LA-A271KS 24V/4A
4. 4K TV: ENVISION P2271WHL
5. Power meter with accumulator: Yokogawa WT210
6. Current probe: TCPA300
7. NETGEAR R7000 1Gbps

Test Environment:

1. Test place: FXN CNSBG Building 1F office
2. Test DUT name: BFX-UA300 DVT V125 board
3. Test environment condition: temperature: 25 deg-C, humidity: 65
4. Test date: 2021/09/02
5. Test result: See section 3 for test results.
6. Test setup picture (block diagram and real test environment picture)

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Test setup picture:



2. Test item and condition

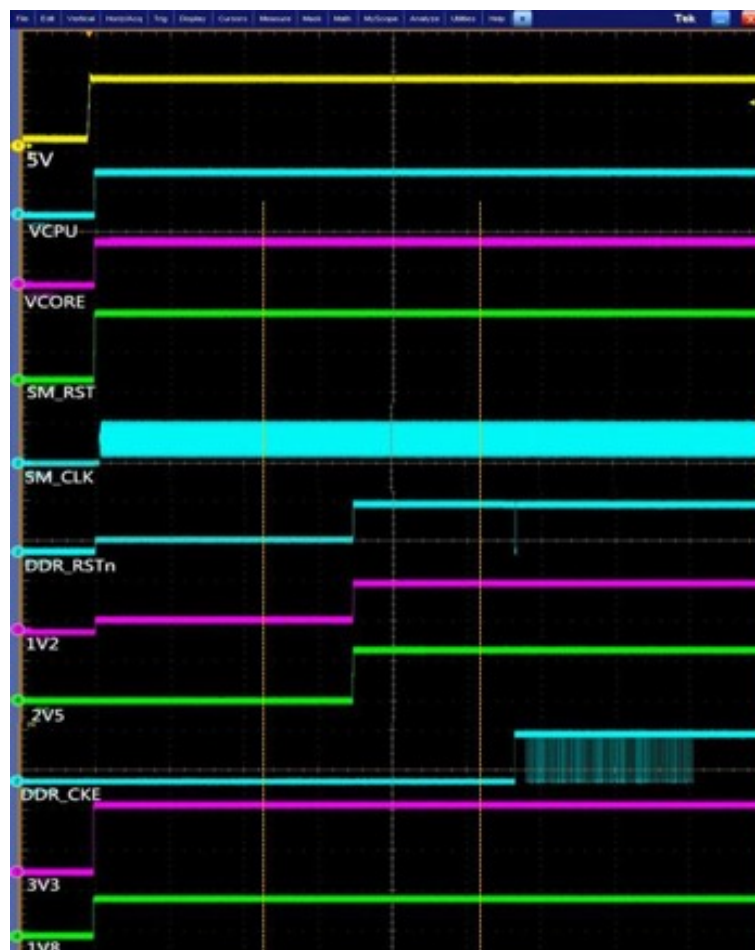
AC power: 220V@60Hz

DC power: 24V/4A

- AC power On/Off
- DC power On/Off
- Standby power On/Off

3. Power on specification

As SOC vendor Synaptic said that due to POR, do not care the timing. The sequence just follow as spec.



	1	2	3	4	5
PWR_3V3					
PWR_1V8					
	SM_RSTI				
		VCORE			
		VCPU			
			DDR_2V5		
				DDR_1V2	

4. Test results:

AC Power on/off Result and Picture

Test Item(Power On)**	Test Result (ms)	Figure	Sequence	Pass/Fail
PWR_5V vs PWR_3V3	1.44	Fig 1.	1	Pass
PWR_5V vs PWR_1V8	1.424	Fig 2.	1	Pass
PWR_5V vs PWR_DDR4_1V2	204.2	Fig 3.	5	Pass
PWR_5V vs SM_RSTIn	0.36	Fig 4.	1	Pass
PWR_5V vs PWR_CPU_1V05*	0.752	Fig 5.	1	Pass
PWR_5V vs PWR_CORE_1V05*	0.816	Fig 6.	1	Pass
PWR_3V3 vs PWR_DDR4_2V5	199.8	Fig 7.	4	Pass
PWR_3V3 vs PWR_VTT_0V6	204.4	Fig 8.	4	Pass

Note:

***: Ask Synaptic SOC vendor, they said the CPU and CORE are no timing limit. So the sequence is ok as currently setup.**

Test Item(Power Off)*	Test Result (ms)	Figure	Sequence	Pass/Fail
PWR_5V vs PWR_3V3	180.6	Fig 9.	TBD	TBD
PWR_5V vs PWR_1V8	142.8	Fig 10.	TBD	TBD
PWR_5V vs PWR_DDR4_1V2	41.8	Fig 11.	TBD	TBD
PWR_5V vs SM_RSTIn	128.4	Fig 12.	TBD	TBD
PWR_5V vs PWR_CPU_1V05*	55.98	Fig 13.	TBD	TBD
PWR_5V vs PWR_CORE_1V05*	52.36	Fig 14.	TBD	TBD
PWR_3V3 vs PWR_DDR4_2V5	6.12	Fig 15.	TBD	TBD
PWR_3V3 vs PWR_VTT_0V6	4.94	Fig 16.	TBD	TBD

Note:

***: Power off does not define, so the measurement is for record.**

The big capacitor of adaptor will discharge to power tree of main board power when AC power off.

AC Power On sequence:

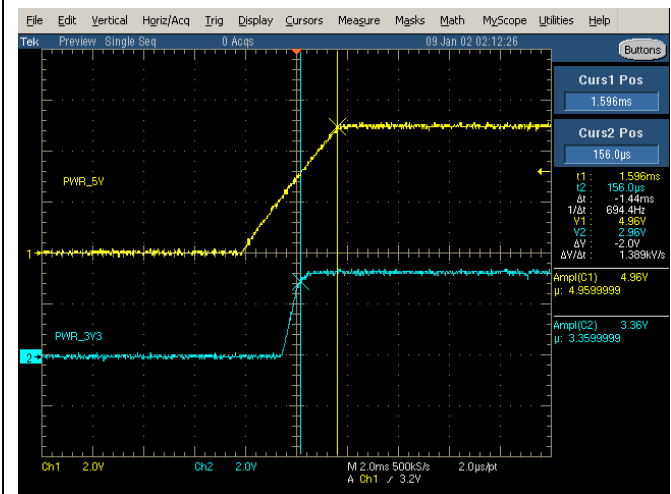


Fig. 1: PWR_5V vs PWR_3V3

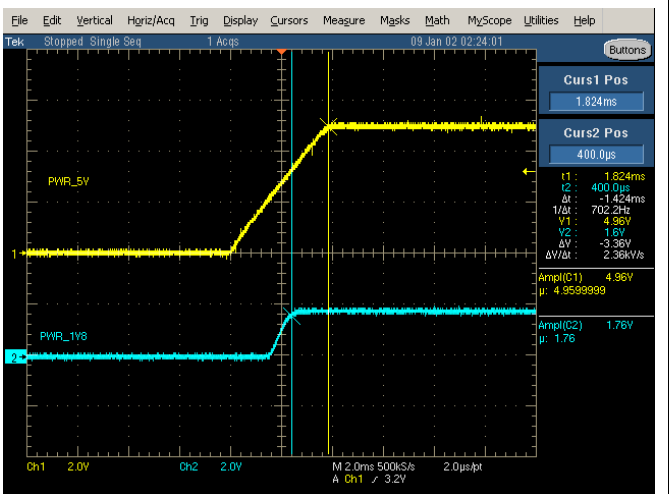


Fig. 2: PWR_5V vs PWR_1V8

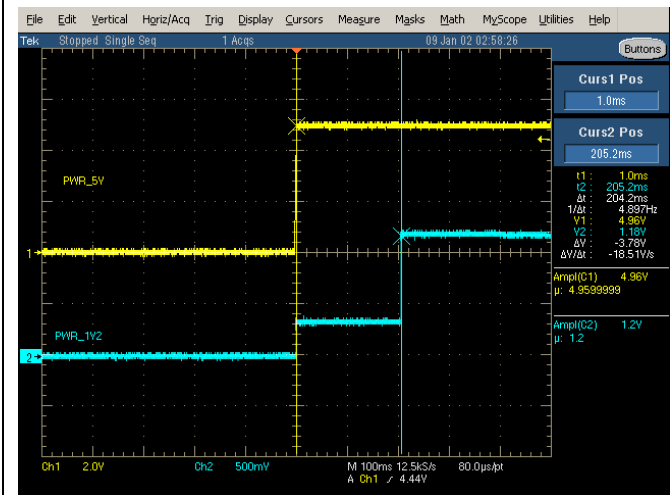


Fig. 3: PWR_5V vs PWR_DDR4_1V2

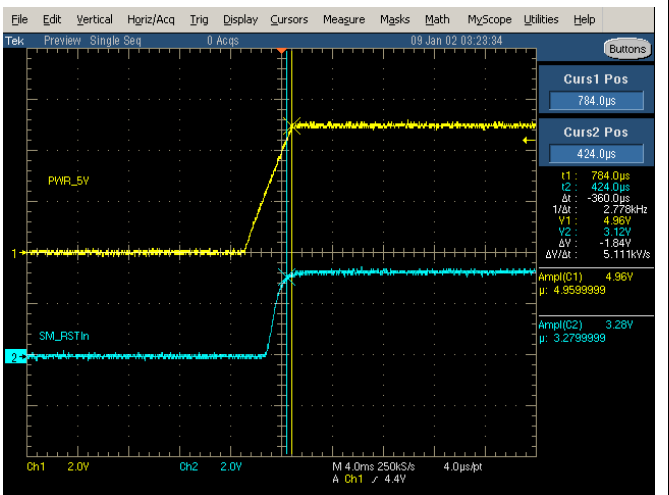


Fig. 4: PWR_5V vs SM_RSTIn

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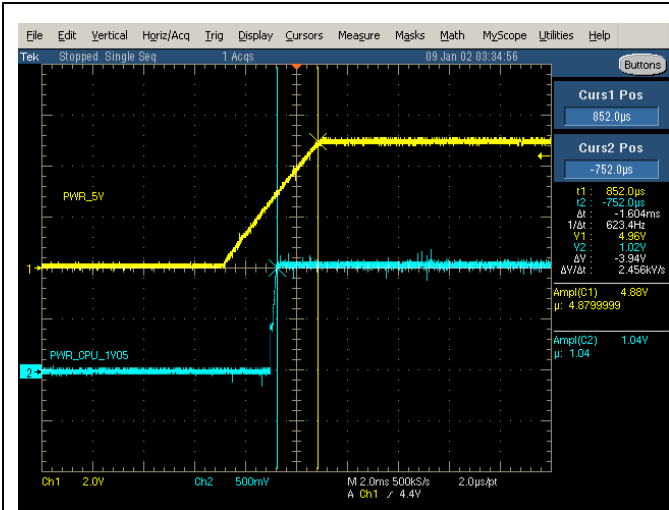


Fig. 5: PWR_5V vs PWR_CPU_1V05

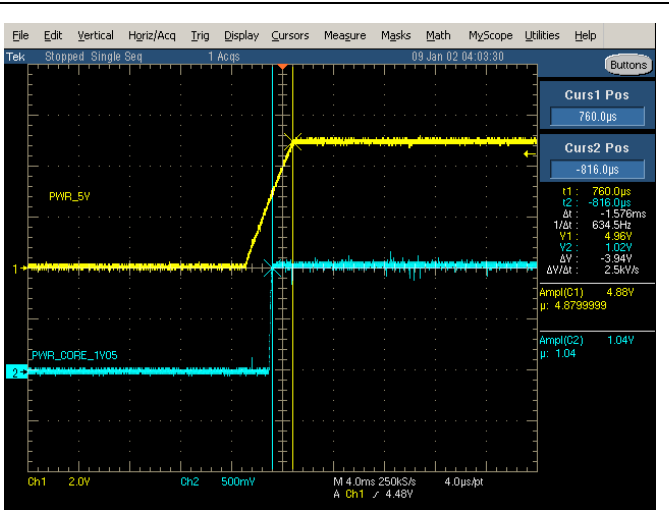


Fig. 6: PWR_5V vs PWR_CORE_1V05

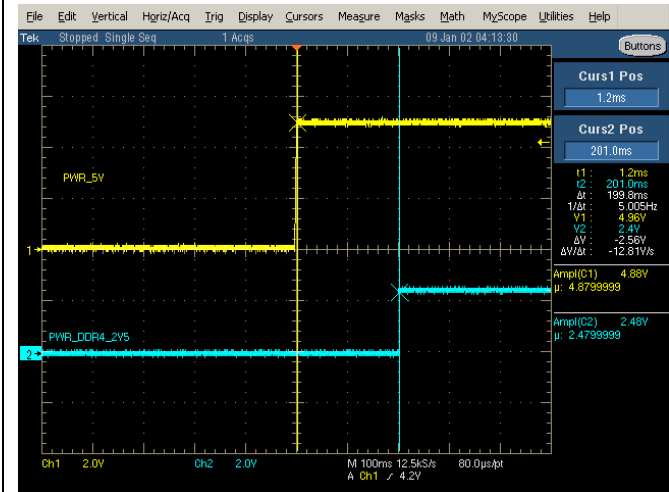


Fig. 7: PWR_3V3 vs PWR_DDR4_2V5

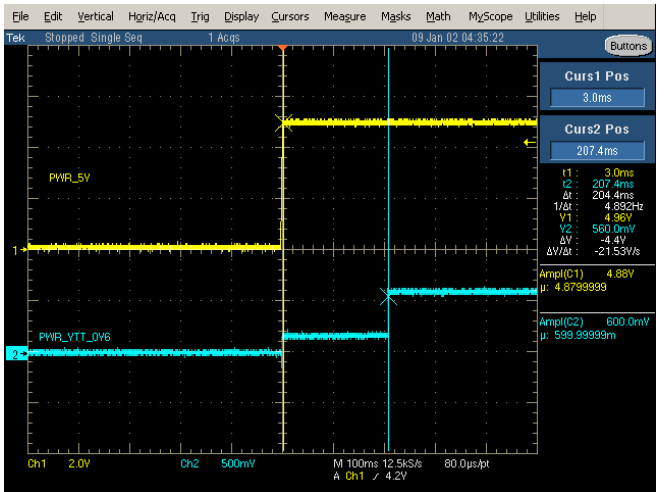


Fig. 8: PWR_3V3 vs PWR_VTT_0V6

AC power off sequence:

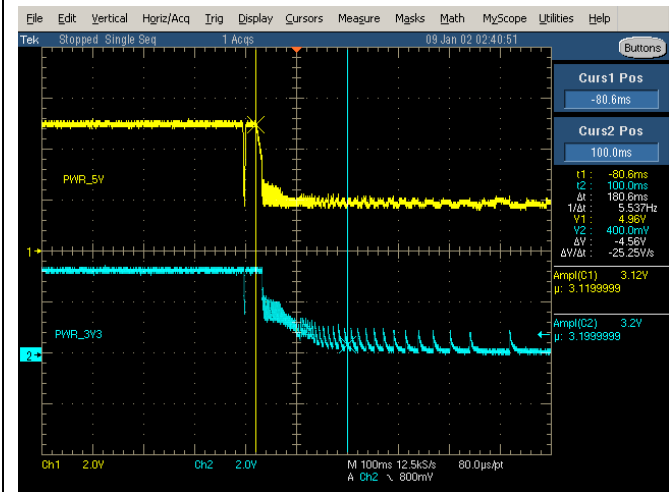


Fig. 9: PWR_5V vs PWR_3V3

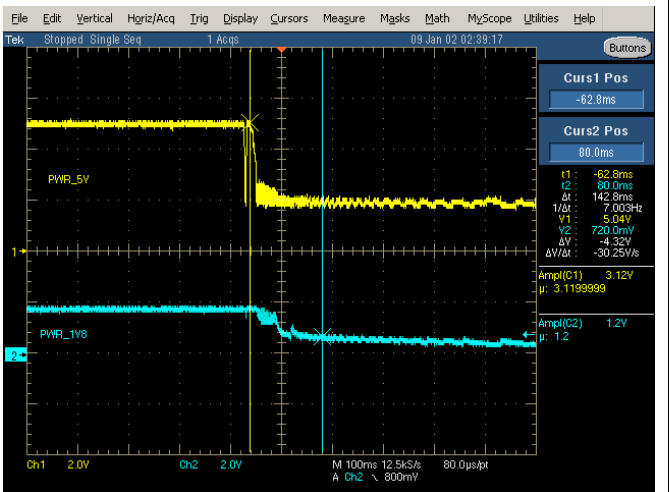


Fig. 10: PWR_5V vs PWR_1V8

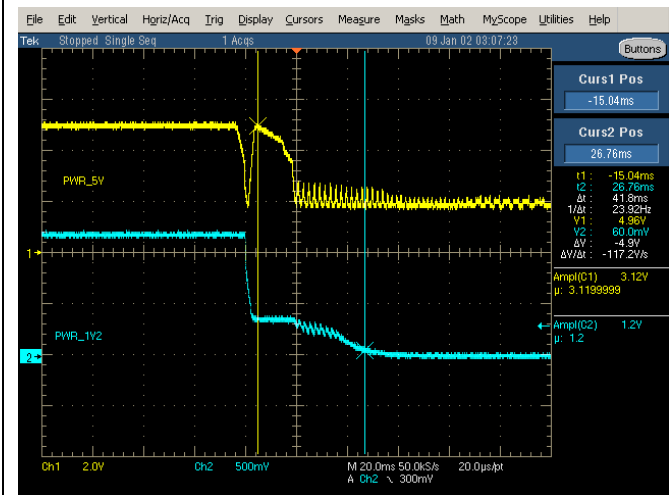


Fig. 11: PWR_5V vs PWR_DDR4_1V2

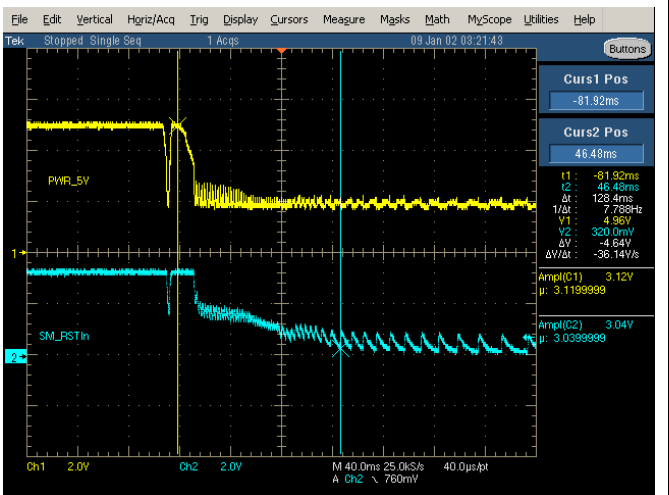


Fig. 12: PWR_5V vs SM_RSTIn

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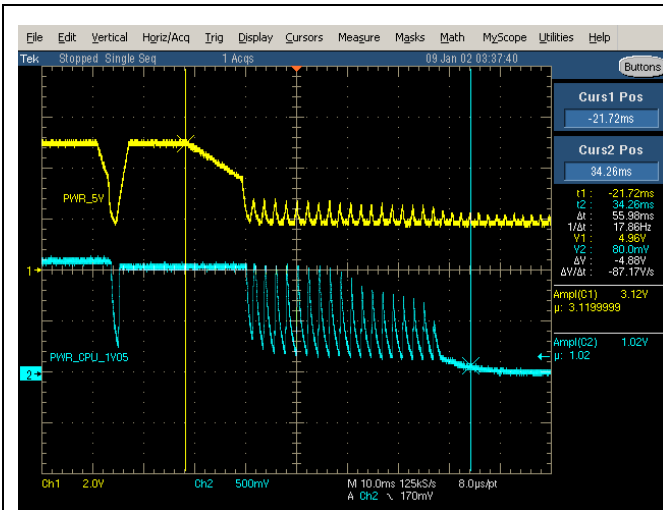


Fig. 13: PWR_5V vs PWR_CPU_1V05

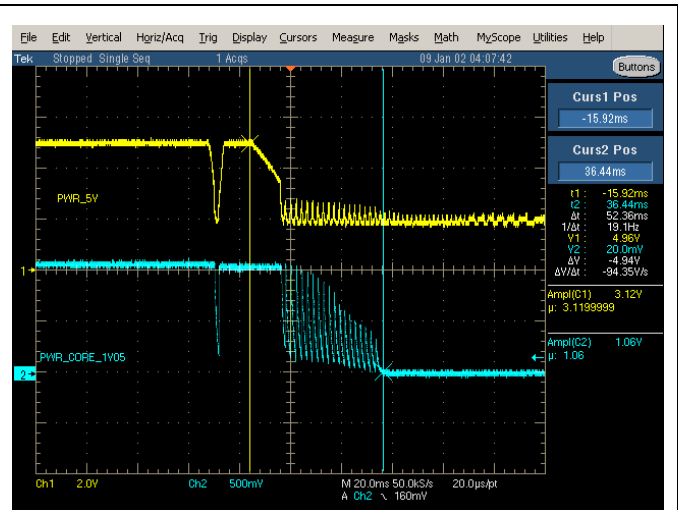


Fig. 14: PWR_5V vs PWR_CORE_1V05

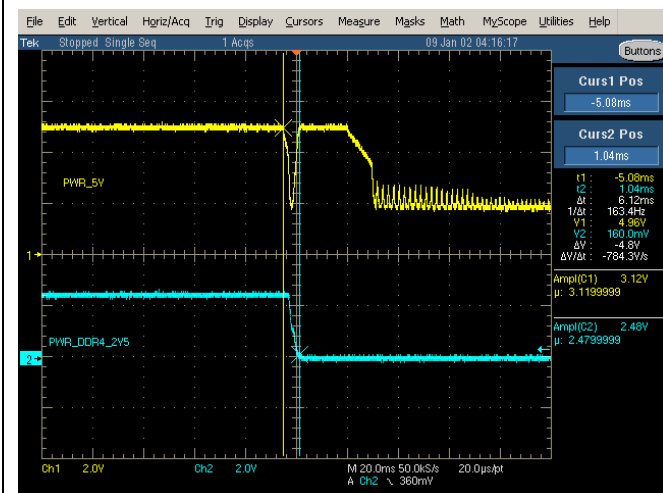


Fig. 15: PWR_3V3 vs PWR_DDR4_2V5

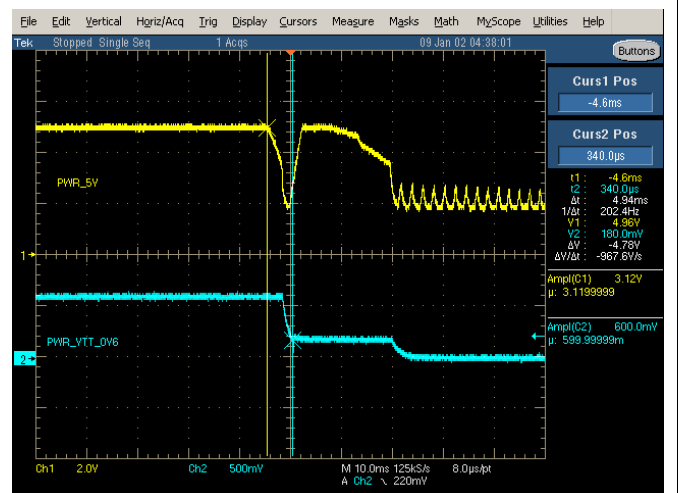


Fig. 16: PWR_3V3 vs PWR_VTT_0V6

DC Power on/off Result and Picture

Test Item(Power On)	Test Result (ms)	Figure	Sequence	Pass/Fail
PWR_5V vs PWR_3V3	1.432	Fig 17.	1	Pass
PWR_5V vs PWR_1V8	1.448	Fig 18.	1	Pass
PWR_5V vs PWR_DDR4_1V2	203.0	Fig 19.	5	Pass
PWR_5V vs SM_RSTIn	0.464	Fig 20.	1	Pass
PWR_5V vs PWR_CPU_1V05*	1.64	Fig 21.	1	Pass
PWR_5V vs PWR_CORE_1V05*	1.528	Fig 22.	1	Pass
PWR_3V3 vs PWR_DDR4_2V5	191.2	Fig 23.	4	Pass
PWR_3V3 vs PWR_VTT_0V6	181	Fig 24.	4	Pass

Note:

***: Ask Synaptic SOC vendor, they said the CPU and CORE are no timing limit. So the sequence is ok as currently setup.**

Test Item(Power Off)*	Test Result (ms)	Figure	Sequence	Pass/Fail
PWR_5V vs PWR_3V3	19.64	Fig 25.	TBD	TBD
PWR_5V vs PWR_1V8	31.92	Fig 26.	TBD	TBD
PWR_5V vs PWR_DDR4_1V2	203	Fig 27.	TBD	TBD
PWR_5V vs SM_RSTIn	0.464	Fig 28.	TBD	TBD
PWR_5V vs PWR_CPU_1V05	1.64	Fig 29.	TBD	TBD
PWR_5V vs PWR_CORE_1V05	1.528	Fig 30.	TBD	TBD
PWR_3V3 vs PWR_DDR4_2V5	191.2	Fig 31.	TBD	TBD
PWR_3V3 vs PWR_VTT_0V6	181	Fig 32.	TBD	TBD

Note:

***: Power off does not define, so the measurement is for record.**

DC power on sequence:

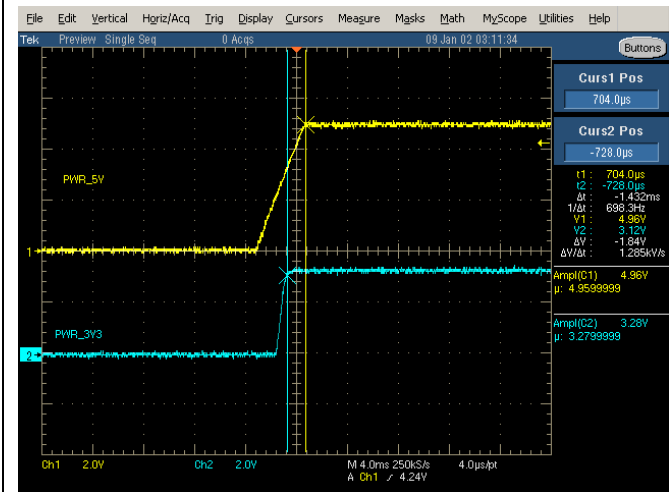


Fig. 17: PWR_5V vs PWR_3V3

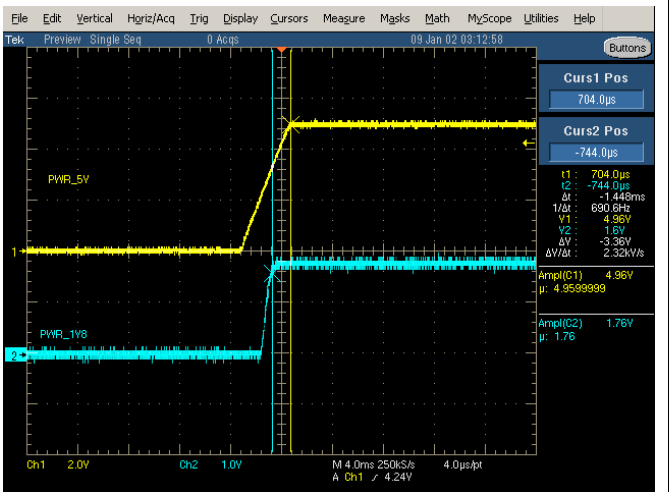


Fig. 18: PWR_5V vs PWR_1V8

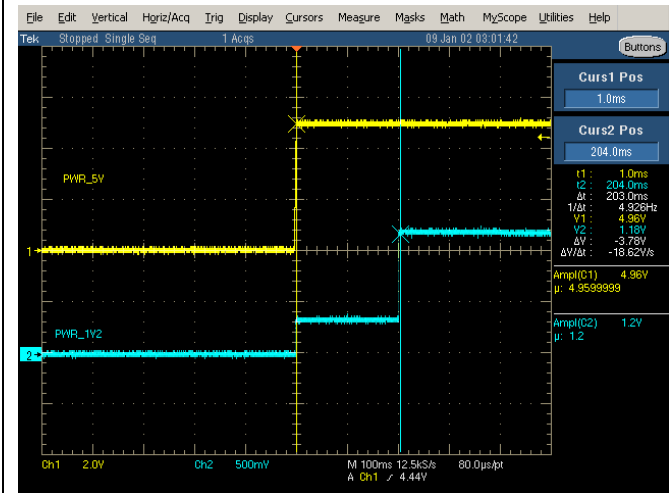


Fig. 19: PWR_5V vs PWR_DDR4_1V2

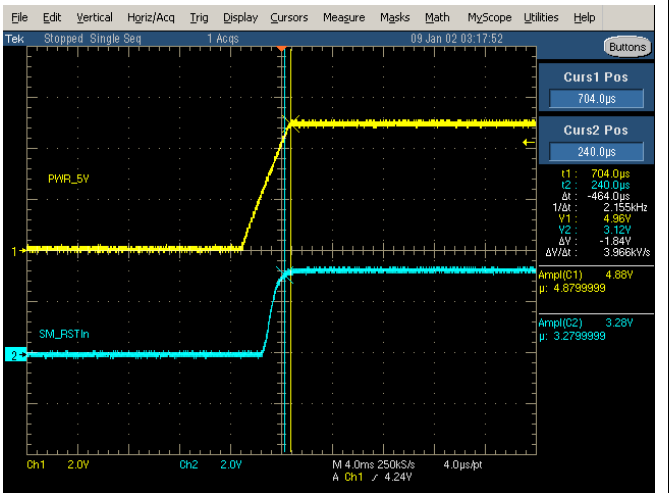


Fig. 20: PWR_5V vs SM_RSTIn

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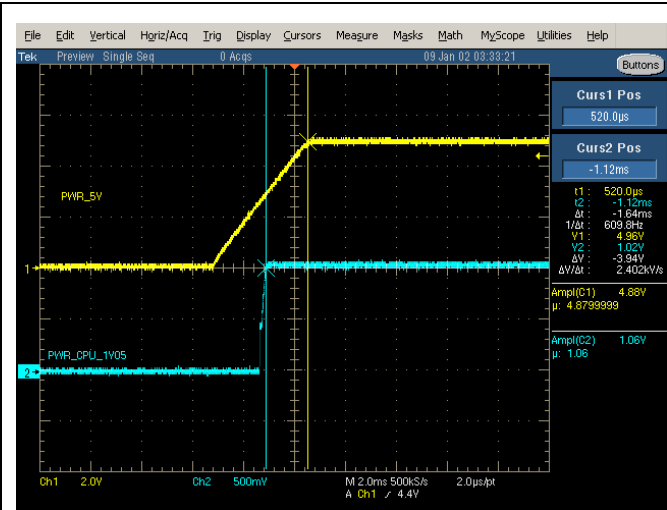


Fig. 21: PWR_5V vs PWR_CPU_1V05

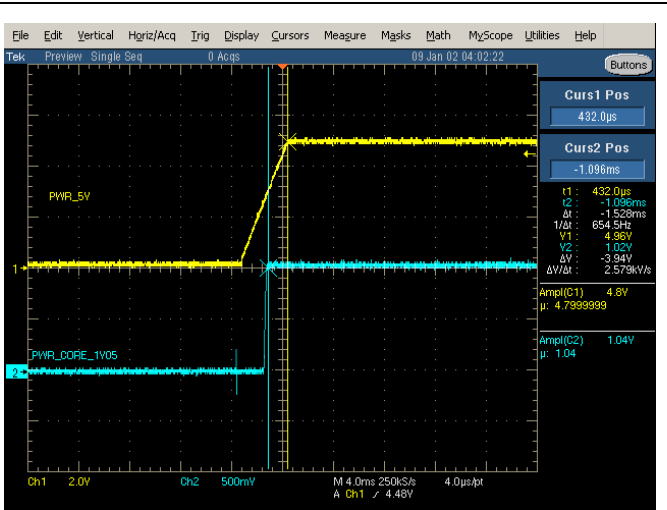


Fig. 22: PWR_5V vs PWR_CORE_1V05

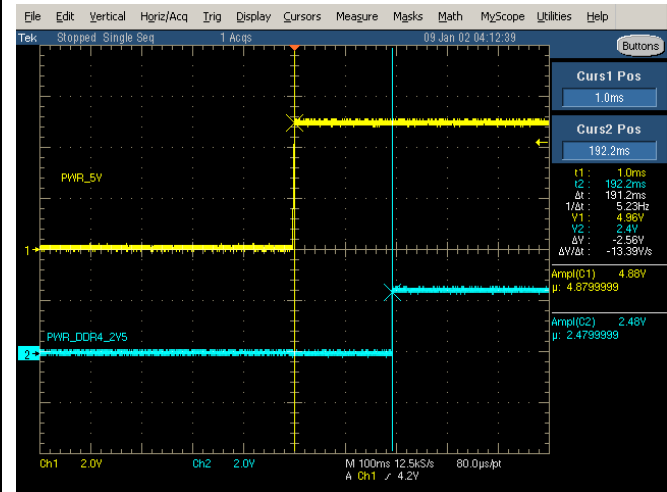


Fig. 23: PWR_3V3 vs PWR_DDR4_2V5

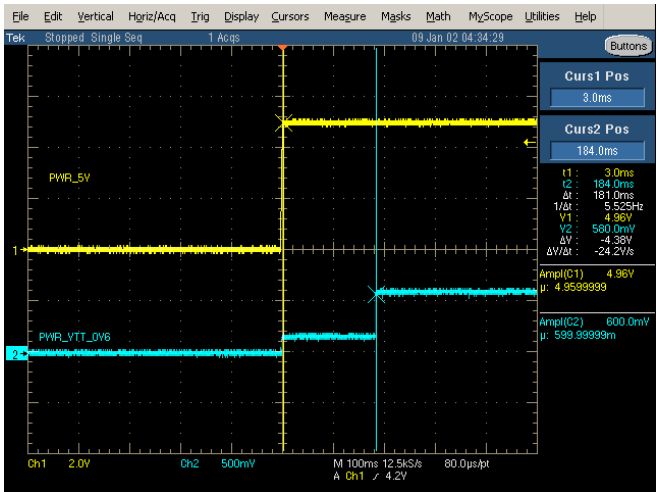


Fig. 24: PWR_3V3 vs PWR_VTT_0V6

DC power off sequence:

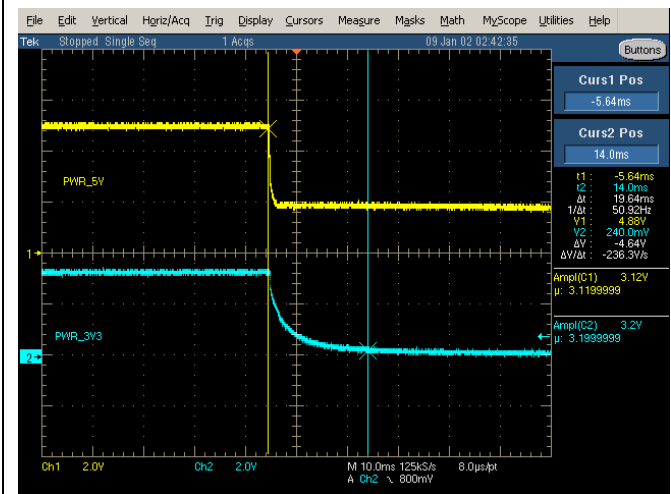


Fig. 25: PWR_5V vs PWR_3V3

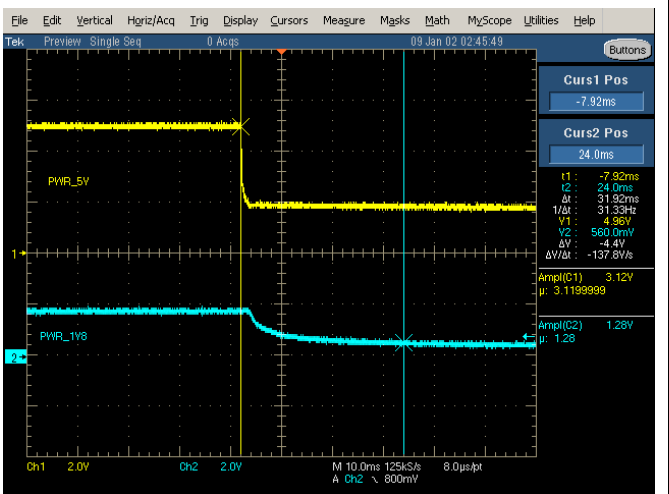


Fig. 26: PWR_5V vs PWR_1V8

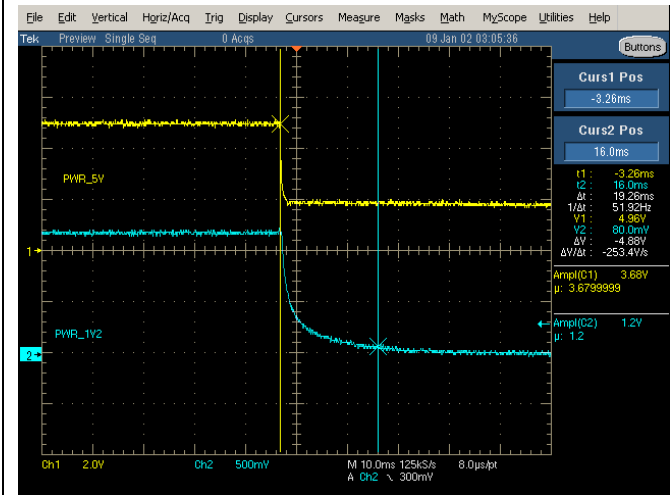


Fig. 27: PWR_5V vs PWR_DDR4_1V2

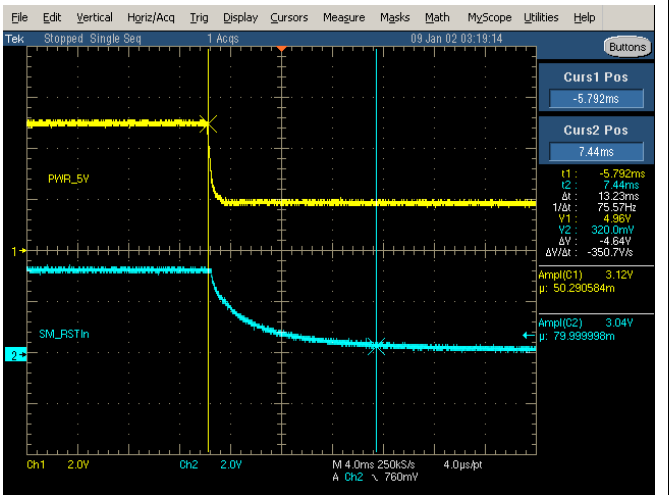


Fig. 28: PWR_5V vs SM_RSTIn

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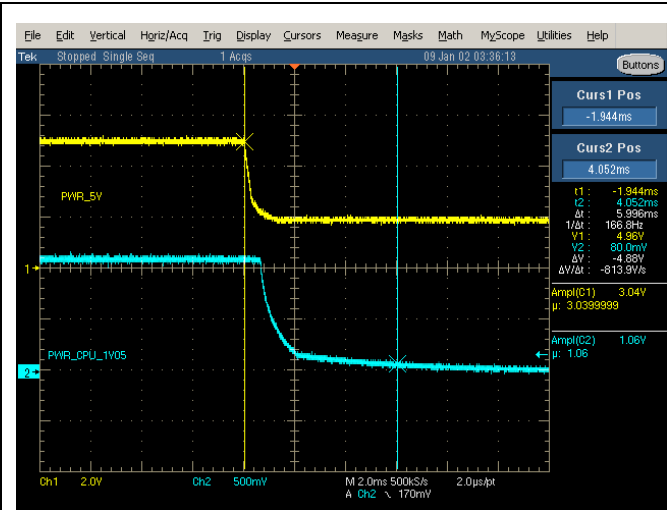


Fig. 29: PWR_5V vs PWR_CPU_1V05

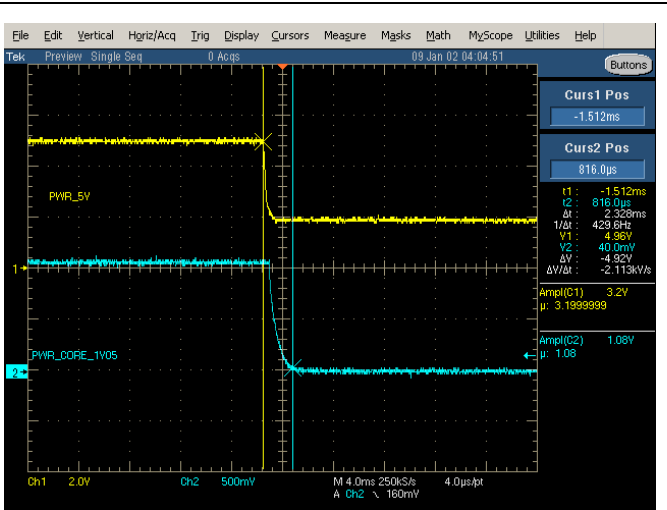


Fig. 30: PWR_5V vs PWR_CORE_1V05

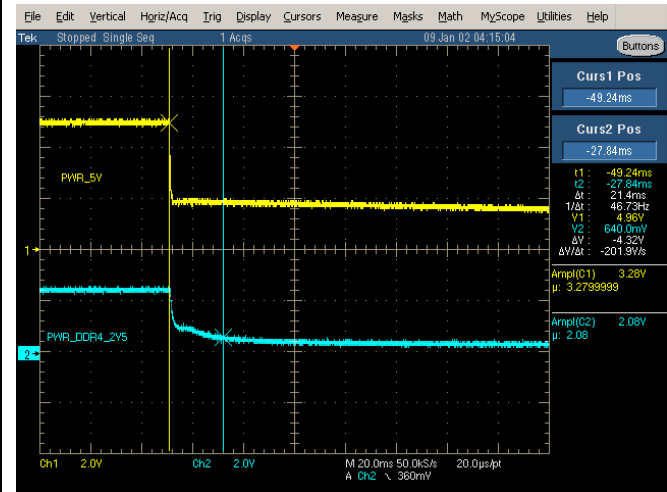


Fig. 31: PWR_3V3 vs PWR_DDR4_2V5

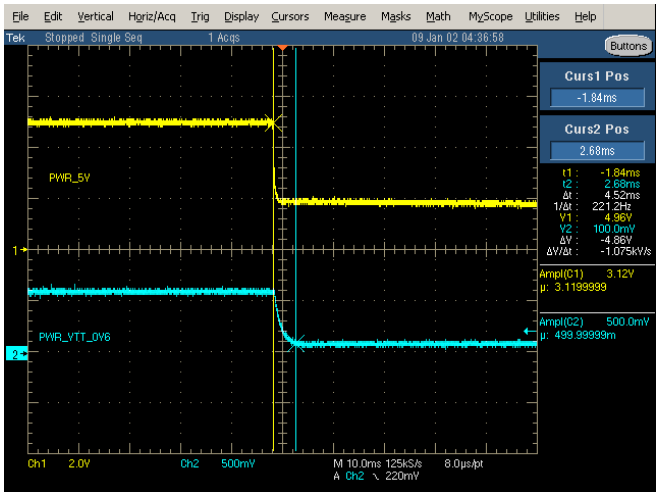


Fig. 32: PWR_3V3 vs PWR_VTT_0V6

Standby Power on/off Result and Picture

Test Item(RCU Power on)*	Test Result (ms)	Figure	Sequence	Pass/Fail
PWR_5V vs PWR_3V3	0	Fig 33.	TBD	TBD
PWR_5V vs PWR_1V8	0	Fig 34.	TBD	TBD
PWR_5V vs PWR_DDR4_1V2	0	Fig 35.	TBD	TBD
PWR_5V vs SM_RSTIn	0	Fig 36.	TBD	TBD
PWR_5V vs PWR_CPU_1V05	0	Fig 37.	TBD	TBD
PWR_5V vs PWR_CORE_1V05	0	Fig 38.	TBD	TBD
PWR_3V3 vs PWR_DDR4_2V5	0	Fig 39.	TBD	TBD
PWR_3V3 vs PWR_VTT_0V6	0	Fig 40.	TBD	TBD

Note:

***: In standby mode, the power tree still cannot be power off. The system will be shutdown and reboot. So the power sequence will no any change.**

Test Item(RCU Power Off)*	Test Result (ms)	Figure	Sequence	Pass/Fail
PWR_5V vs PWR_3V3	0	Fig 41.	TBD	TBD
PWR_5V vs PWR_1V8	0	Fig 42.	TBD	TBD
PWR_5V vs PWR_DDR4_1V2	0	Fig 43.	TBD	TBD
PWR_5V vs SM_RSTIn	0	Fig 44.	TBD	TBD
PWR_5V vs PWR_CPU_1V05*	0	Fig 45.	TBD	TBD
PWR_5V vs PWR_CORE_1V05*	0	Fig 46.	TBD	TBD
PWR_3V3 vs PWR_DDR4_2V5	0	Fig 47.	TBD	TBD
PWR_3V3 vs PWR_VTT_0V6	0	Fig 48.	TBD	TBD

Note:

***: In standby mode, the power tree still cannot be power off. The system will be shutdown and reboot. So the power sequence will no any change.**

Standby power of sequence:

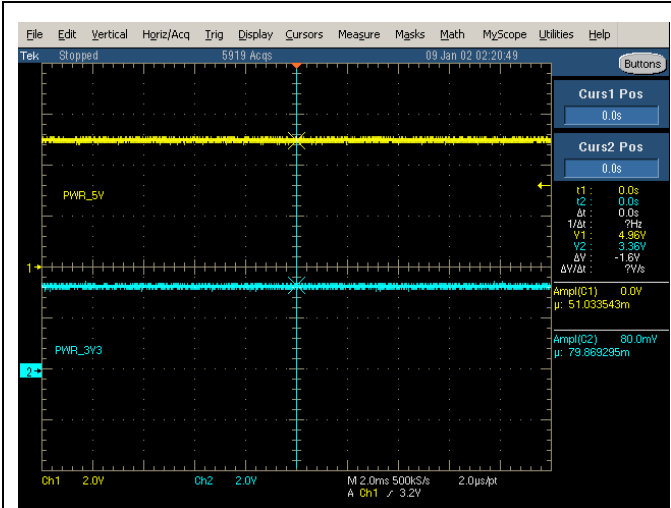


Fig. 33: PWR_5V vs PWR_3V3

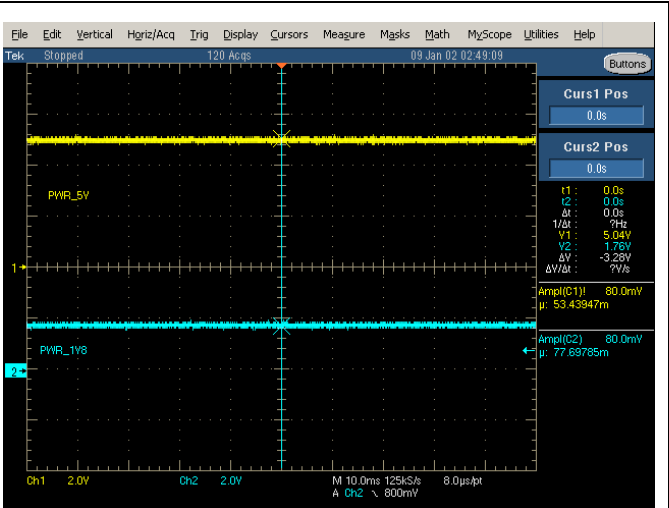


Fig. 34: PWR_5V vs PWR_1V8

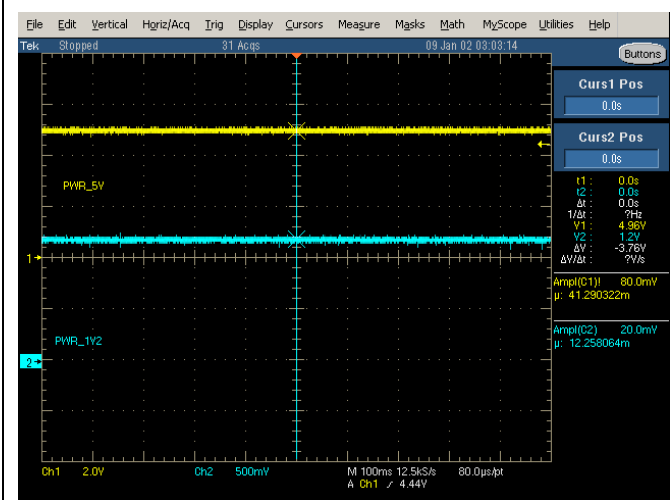


Fig. 35: PWR_5V vs PWR_DDR4_1V2

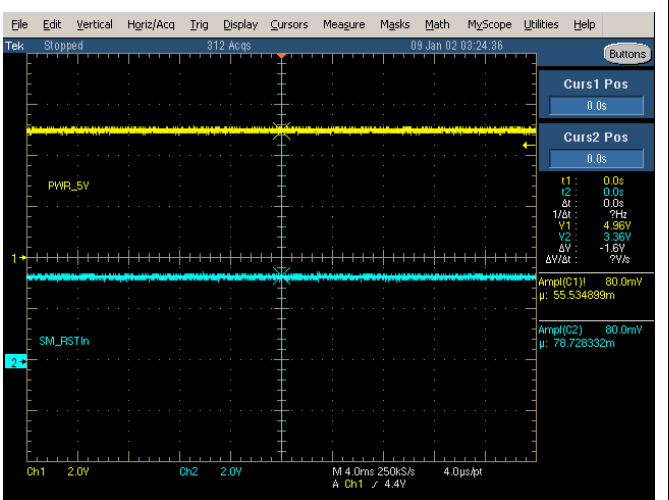


Fig. 36: PWR_5V vs SM_RSTIn

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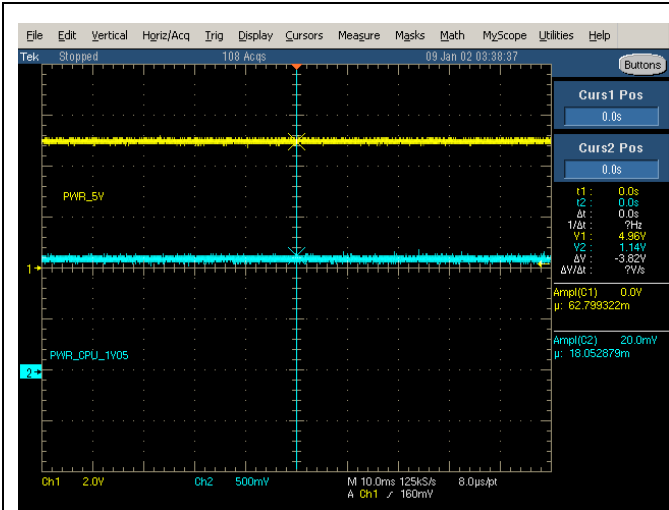


Fig. 37: PWR_5V vs PWR_CPU_1V05

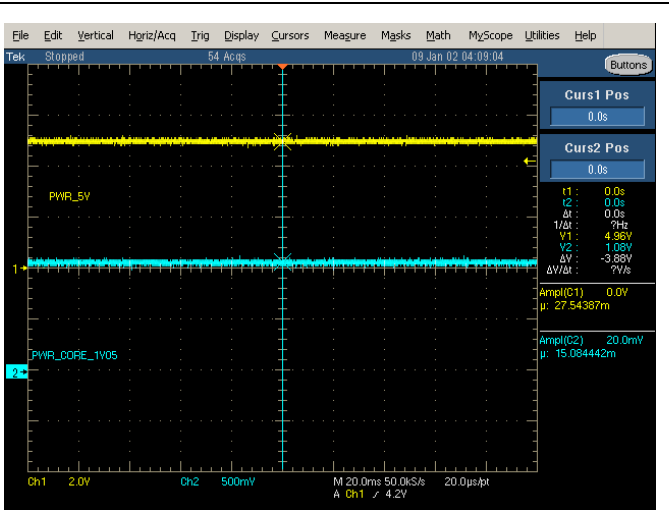


Fig. 38: PWR_5V vs PWR_CORE_1V05

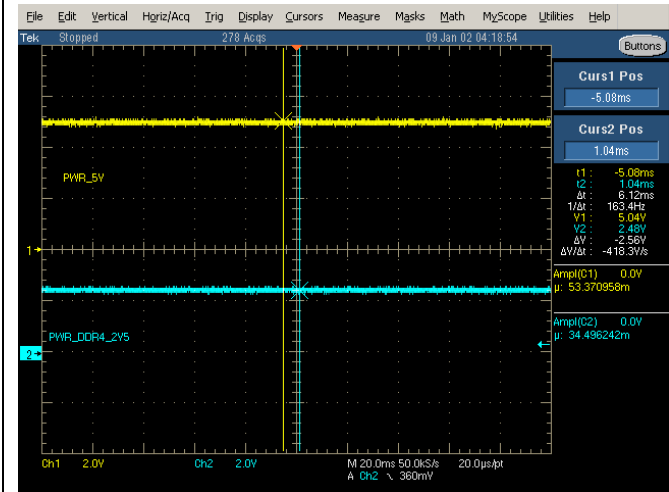


Fig. 39: PWR_3V3 vs PWR_DDR4_2V5

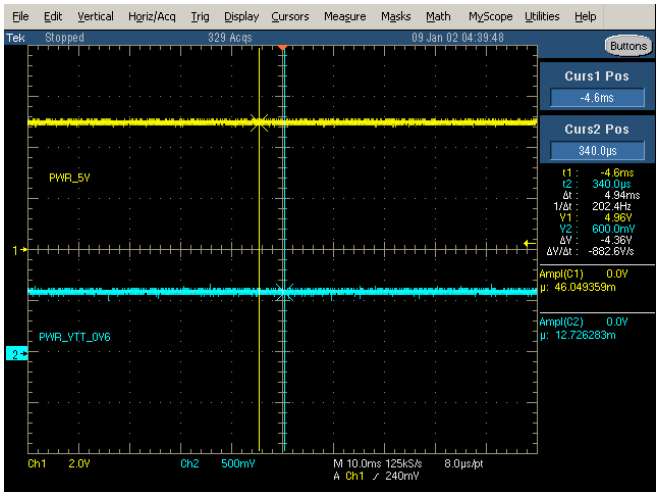


Fig. 40: PWR_3V3 vs PWR_VTT_0V6

Standby power off sequence:

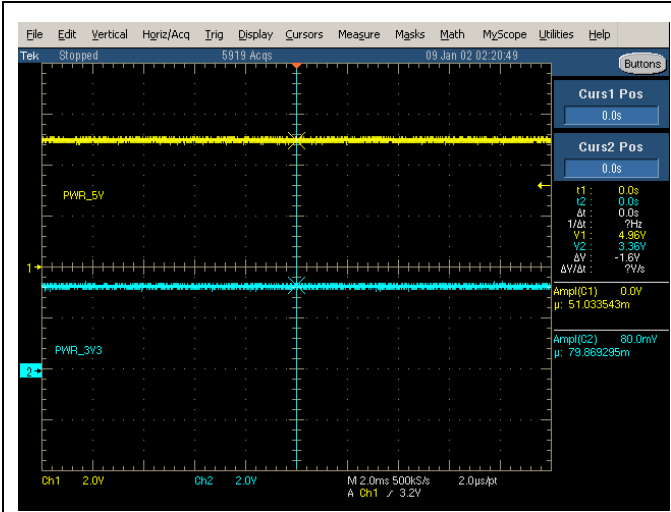


Fig. 41: PWR_5V vs PWR_3V3

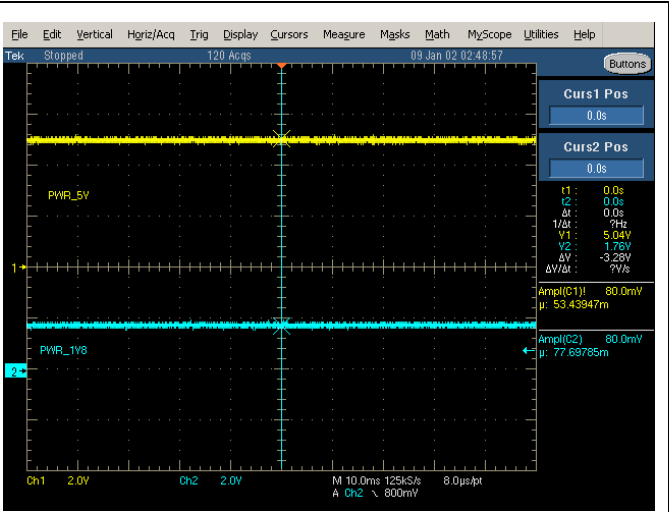


Fig. 42: PWR_5V vs PWR_1V8

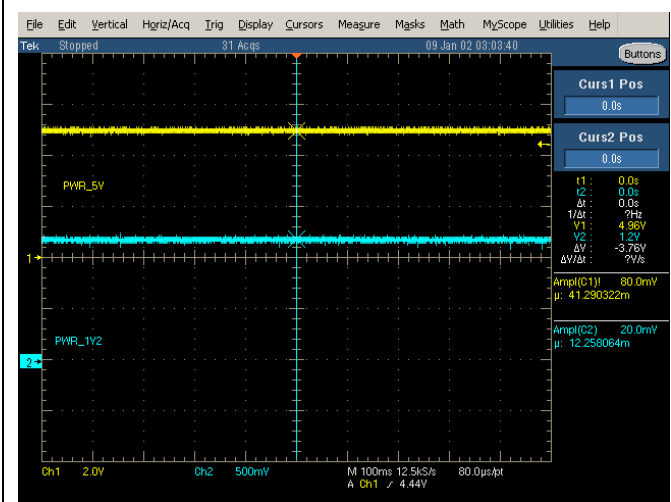


Fig. 43: PWR_5V vs PWR_DDR4_1V2

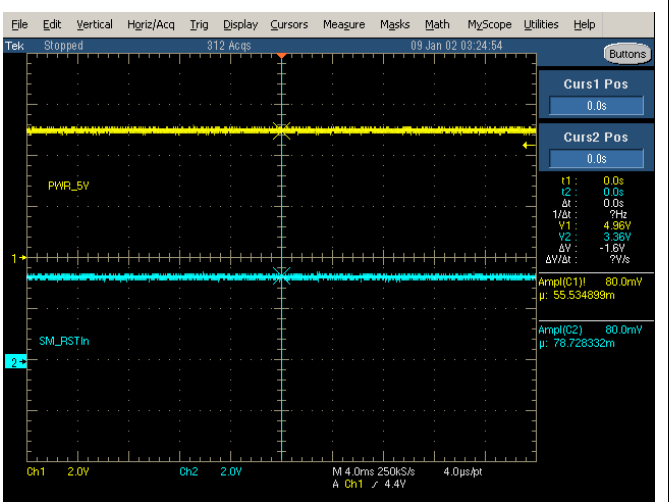


Fig. 44: PWR_5V vs SM_RSTIn

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Fig. 45: PWR_5V vs PWR_CPU_1V05

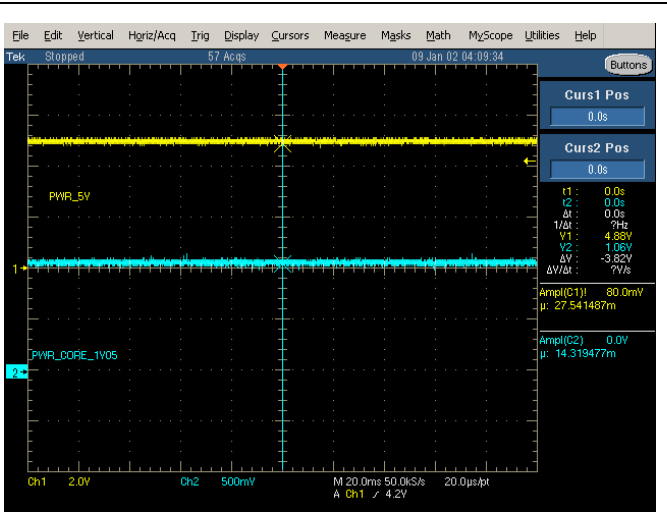


Fig. 46: PWR_5V vs PWR_CORE_1V05

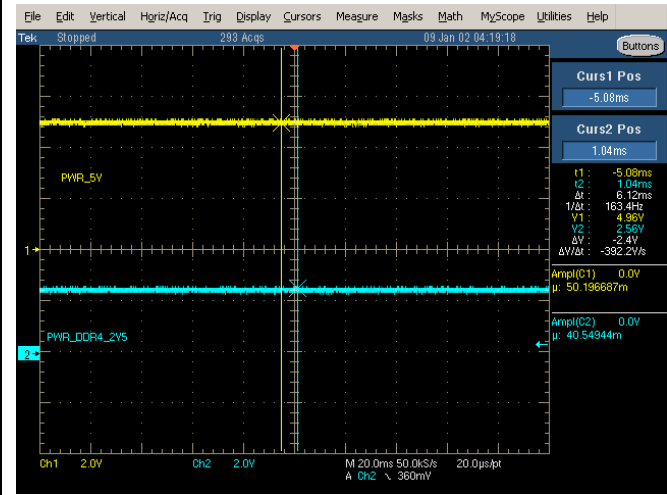


Fig. 47: PWR_3V3 vs PWR_DDR4_2V5

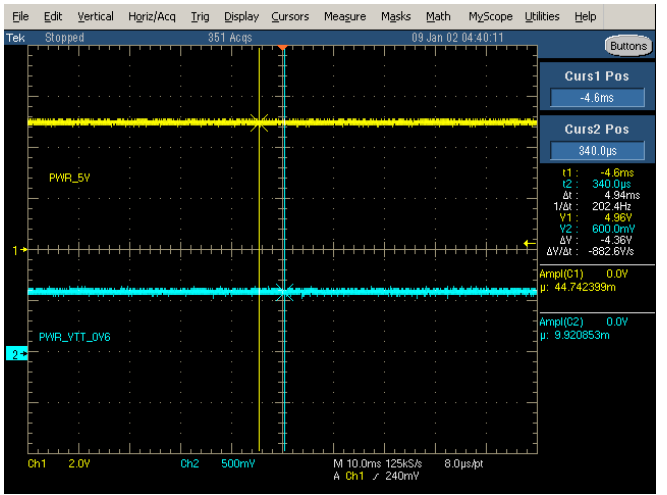


Fig. 48: PWR_3V3 vs PWR_VTT_0V6